

## EXHIBIT 036

**U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)**

“Integrated circuit with data communication network and IC design method”

'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>
1. An integrated circuit comprising:	<p>Without conceding that the preamble of claim 1 of the '2893 Patent is limiting, the Motorola Edge+ Gen 2 (hereinafter, the "Motorola product") includes an integrated circuit.</p> <p>For example, the Motorola product includes the Qualcomm Snapdragon 8 Gen 1 Mobile Platform system on chip (hereinafter, the "Snapdragon SoC").</p> <div data-bbox="502 584 952 1068"> </div> <div data-bbox="1106 567 1710 633"> <h2>Motorola Edge+ Gen 2</h2> </div> <div data-bbox="1106 649 1681 680"> <p>Featuring a Snapdragon 8 Gen 1 Mobile Platform</p> </div> <div data-bbox="1106 703 1841 992"> <p>The Motorola edge+ was born for 5G speed. This state-of-the-art smartphone gives you up to 2 full days of power, lightning-fast speed, and pro-quality features for doing more of what you love. Leave lag time behind with a massive 256 GB+ memory and blazing-fast premium Snapdragon mobile platform. Enjoy days of entertainment on a beautiful display that wraps around the edges and has superior stereo-quality sound. Get the best of Android OS without the extra baggage.</p> </div> <div data-bbox="1148 1093 1258 1116"> <a href="#">Learn more</a> </div> <div data-bbox="460 1179 1624 1217"> <p><a href="https://www.qualcomm.com/snapdragon/device-finder/motorola-edge--gen-2">https://www.qualcomm.com/snapdragon/device-finder/motorola-edge--gen-2</a></p> </div>

<sup>1</sup> The Motorola product is charted as a representative product made used, sold, offered for sale, and/or imported by Motorola. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

**U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)**  
**"Integrated circuit with data communication network and IC design method"**

'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>			
a plurality of functional blocks; and	<p>The Snapdragon SoC included in the Motorola product includes a plurality of functional blocks, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment &amp; Services, Secure Processing Unit (SPU):</p> <div style="display: flex; align-items: center;">  <div style="margin-left: 10px;"> <p><b>Snapdragon</b> 8 mobile platform Gen 1</p> </div> <div style="flex-grow: 1; text-align: right; margin-right: 20px;"> <p>SPECIFICATIONS &amp; FEATURES</p> </div> </div> <table border="0" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%; vertical-align: top;"> <p><b>Artificial Intelligence</b></p> <hr/>           Qualcomm® Adreno™ GPU            Qualcomm® Kryo™ CPU            Qualcomm® Hexagon™ Processor           <ul style="list-style-type: none"> <li>• Fused AI Accelerator               <ul style="list-style-type: none"> <li>• Hexagon Tensor Accelerator</li> <li>• Hexagon Vector eXtensions</li> <li>• Hexagon Scalar Accelerator</li> </ul> </li> <li>• Support for mix precision(INT8+INT16)</li> <li>• Support for all precisions (INT8, INT16, FP16)</li> </ul> <hr/>           Qualcomm® Sensing Hub         </td> <td style="width: 33%; vertical-align: top;"> <p><b>Camera</b></p> <hr/>           Qualcomm Spectra™ Image Signal Processor           <ul style="list-style-type: none"> <li>• Triple 18-bit ISPs</li> <li>• Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP)</li> <li>• Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 200 Megapixel Photo Capture</li> </ul> <hr/>           Rec. 2020 color gamut photo and video capture            Up to 10-bit color depth photo and video capture            8K HDR Video Capture + 64 MP Photo Capture         </td> <td style="width: 33%; vertical-align: top;"> <p><b>CPU</b></p> <hr/>           Kryo CPU           <ul style="list-style-type: none"> <li>• Up to 3.0 GHz*, with Arm Cortex-X2 technology</li> <li>• 64-bit Architecture</li> </ul> <p><b>Visual Subsystem</b></p> <hr/>           Adreno GPU           <ul style="list-style-type: none"> <li>• Vulkan® 1.1 API support</li> <li>• HDR gaming (10-bit color depth, Rec. 2020 color gamut)</li> <li>• Physically Based Rendering</li> <li>• Volumetric Rendering</li> <li>• Adreno Frame Motion Engine</li> <li>• API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1</li> <li>• Hardware-accelerated H.265 and VP9 decoder</li> <li>• HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision</li> </ul> <p><b>Security</b></p> <hr/>           Platform Security Foundations, Trusted Execution Environment &amp; Services, Secure Processing Unit (SPU)           <hr/>           Trust Management Engine           <hr/>           Qualcomm® wireless edge services (WES) and premium security features           <hr/>           Qualcomm® 3D Sonic Sensor and Qualcomm 3D Sonic Max (fingerprint sensor)           <hr/>           Qualcomm® Type-1 Hypervisor         </td> </tr> </table>	<p><b>Artificial Intelligence</b></p> <hr/> Qualcomm® Adreno™ GPU Qualcomm® Kryo™ CPU Qualcomm® Hexagon™ Processor <ul style="list-style-type: none"> <li>• Fused AI Accelerator               <ul style="list-style-type: none"> <li>• Hexagon Tensor Accelerator</li> <li>• Hexagon Vector eXtensions</li> <li>• Hexagon Scalar Accelerator</li> </ul> </li> <li>• Support for mix precision(INT8+INT16)</li> <li>• Support for all precisions (INT8, INT16, FP16)</li> </ul> <hr/> Qualcomm® Sensing Hub	<p><b>Camera</b></p> <hr/> Qualcomm Spectra™ Image Signal Processor <ul style="list-style-type: none"> <li>• Triple 18-bit ISPs</li> <li>• Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP)</li> <li>• Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 200 Megapixel Photo Capture</li> </ul> <hr/> Rec. 2020 color gamut photo and video capture Up to 10-bit color depth photo and video capture 8K HDR Video Capture + 64 MP Photo Capture	<p><b>CPU</b></p> <hr/> Kryo CPU <ul style="list-style-type: none"> <li>• Up to 3.0 GHz*, with Arm Cortex-X2 technology</li> <li>• 64-bit Architecture</li> </ul> <p><b>Visual Subsystem</b></p> <hr/> Adreno GPU <ul style="list-style-type: none"> <li>• Vulkan® 1.1 API support</li> <li>• HDR gaming (10-bit color depth, Rec. 2020 color gamut)</li> <li>• Physically Based Rendering</li> <li>• Volumetric Rendering</li> <li>• Adreno Frame Motion Engine</li> <li>• API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1</li> <li>• Hardware-accelerated H.265 and VP9 decoder</li> <li>• HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision</li> </ul> <p><b>Security</b></p> <hr/> Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU) <hr/> Trust Management Engine <hr/> Qualcomm® wireless edge services (WES) and premium security features <hr/> Qualcomm® 3D Sonic Sensor and Qualcomm 3D Sonic Max (fingerprint sensor) <hr/> Qualcomm® Type-1 Hypervisor
<p><b>Artificial Intelligence</b></p> <hr/> Qualcomm® Adreno™ GPU Qualcomm® Kryo™ CPU Qualcomm® Hexagon™ Processor <ul style="list-style-type: none"> <li>• Fused AI Accelerator               <ul style="list-style-type: none"> <li>• Hexagon Tensor Accelerator</li> <li>• Hexagon Vector eXtensions</li> <li>• Hexagon Scalar Accelerator</li> </ul> </li> <li>• Support for mix precision(INT8+INT16)</li> <li>• Support for all precisions (INT8, INT16, FP16)</li> </ul> <hr/> Qualcomm® Sensing Hub	<p><b>Camera</b></p> <hr/> Qualcomm Spectra™ Image Signal Processor <ul style="list-style-type: none"> <li>• Triple 18-bit ISPs</li> <li>• Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP)</li> <li>• Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag</li> <li>• Up to 200 Megapixel Photo Capture</li> </ul> <hr/> Rec. 2020 color gamut photo and video capture Up to 10-bit color depth photo and video capture 8K HDR Video Capture + 64 MP Photo Capture	<p><b>CPU</b></p> <hr/> Kryo CPU <ul style="list-style-type: none"> <li>• Up to 3.0 GHz*, with Arm Cortex-X2 technology</li> <li>• 64-bit Architecture</li> </ul> <p><b>Visual Subsystem</b></p> <hr/> Adreno GPU <ul style="list-style-type: none"> <li>• Vulkan® 1.1 API support</li> <li>• HDR gaming (10-bit color depth, Rec. 2020 color gamut)</li> <li>• Physically Based Rendering</li> <li>• Volumetric Rendering</li> <li>• Adreno Frame Motion Engine</li> <li>• API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1</li> <li>• Hardware-accelerated H.265 and VP9 decoder</li> <li>• HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision</li> </ul> <p><b>Security</b></p> <hr/> Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU) <hr/> Trust Management Engine <hr/> Qualcomm® wireless edge services (WES) and premium security features <hr/> Qualcomm® 3D Sonic Sensor and Qualcomm 3D Sonic Max (fingerprint sensor) <hr/> Qualcomm® Type-1 Hypervisor		

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	<p><b>Wi-Fi &amp; Bluetooth*</b></p> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> <li>Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), Wi-Fi 5 (802.11ac), 802.11a/b/g/n</li> <li>Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz, 6 GHz</li> <li>Peak speed: 3.6 Gbps</li> <li>Channel Bandwidth: 20/40/80/160 MHz</li> <li>8-stream sounding (for 8x8 MU-MIMO)</li> <li>MIMO Configuration: 2x2 (2-stream)</li> <li>MU-MIMO (Uplink &amp; Downlink)</li> <li>4K QAM</li> <li>OFDMA (Uplink &amp; Downlink)</li> <li>Dual-band simultaneous (2x2 + 2x2)</li> <li>Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal</li> </ul> <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> <li>Bluetooth Features: Bluetooth 5.2, LE Audio, Dual Bluetooth antennas</li> <li>Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio</li> </ul> <p><a href="http://snapdragon.com">snapdragon.com</a></p> <div style="background-color: black; color: white; padding: 10px; font-size: small;"> <p>* Exact speed measured at 2.995 GHz      Certain optional features available subject to carrier and OEM selection for an additional fee.      Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Smart Transmit, Qualcomm Wideband Envelope, Qualcomm AI Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Aqstic, Qualcomm 3D Sonic Sensor, Qualcomm Type 1 Hypervisor, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries.      Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kryo, Smart Transmit, Qualcomm Spectra, Qualcomm Aqstic, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd.      ©2021 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</p> </div> <p><a href="https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/snapdragon-8-gen-1-mobile-platform-product-brief.pdf">https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/snapdragon-8-gen-1-mobile-platform-product-brief.pdf</a></p>
a data communication network comprising a plurality of	The Snapdragon SoC included in the Motorola product includes a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents.

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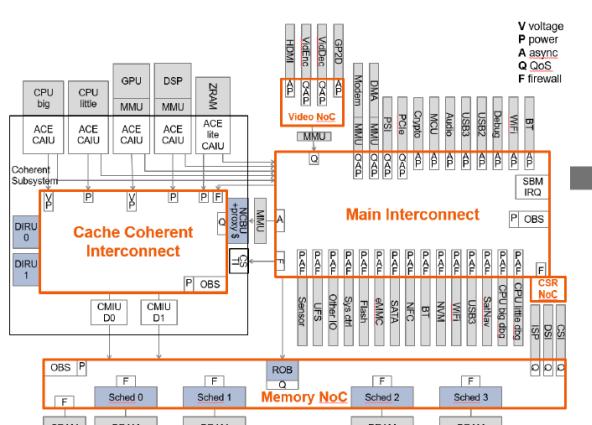
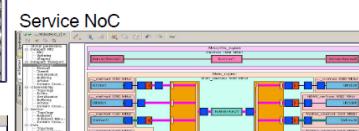
“Integrated circuit with data communication network and IC design method”

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network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,	<p>The Snapdragon SoC included in the Motorola product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) as a data communication network:</p> <div data-bbox="481 453 1030 1139" style="border: 1px solid #ccc; padding: 10px; text-align: center;"><p>Qualcomm</p><p></p><p>Arteris-developed NoC technology is the backbone of <b>Snapdragon application processors &amp; LTE modems</b>, Atheros wireless connectivity SoCs, and CSR IoT products.</p><p><a href="#" style="border: 1px solid orange; padding: 2px 10px; color: orange;">LEARN MORE »</a></p></div> <p><a href="https://web.archive.org/web/20210514110614/https://www.arteris.com/customers">https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</a></p>

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	<p>Certain Arteris Technology Assets Acquired</p> <p>by <b>Kurt Shuler</b>, on October 31, 2013</p> <p>Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p>SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial <b>network-on-chip (NoC) interconnect IP</b> solutions, today announced that Qualcomm Technologies, Inc. ("Qualcomm"), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p><b>“Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris' Network-on-Chip interconnect IP technology.”</b></p> <p style="text-align: center;"><b>ARTERIS IP</b></p> <p style="text-align: center;"><small>K. Charles Janac, President and CEO, Arteris</small></p> <p><a href="https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31">https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31</a>; <a href="https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team">https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</a></p> <p>A large SoC, such as the Snapdragon SoC included in the Motorola product may include multiple classes of Arteris NoC data communication network:</p>

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	<h2 style="color: red; text-align: center;">Logical Interconnect Topology Development</h2> <p style="text-align: center;">FLEXNOC &amp; NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p>  <div style="display: flex; justify-content: space-around;"> <div style="width: 45%;"> <p><b>Main NoC</b></p>  </div> <div style="width: 45%;"> <p><b>Ncore Cache Coherent NoC</b></p>  </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 10px;"> <div style="width: 45%;"> <p><b>Service NoC</b></p>  </div> <div style="width: 45%;"> <p><b>Memory NoC</b></p>  </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 10px;"> <div style="width: 45%;"> <p><b>Video NoC</b></p>  </div> </div> <ul style="list-style-type: none"> <li>• ArChip16 Example: Large SoCs have multiple classes of interconnect             <ul style="list-style-type: none"> <li>– Non-coherent, Coherent, Control/Status, Observability, etc.</li> </ul> </li> <li>• Ncore &amp; FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility</li> </ul> <p style="text-align: center; font-size: small; margin-top: 20px;"> <span style="margin-right: 100px;">ARTERIS IP</span> <span>ISPD 2018, 28 March 2018</span> <span>Copyright © 2018 Arteris IP   9</span> </p> <p style="text-align: center; margin-top: 20px;"> <i>See Physical Interconnect Aware Network Optimizer, <a href="http://www.ispd.cc/slides/2018/s7_2.pdf">http://www.ispd.cc/slides/2018/s7_2.pdf</a>, at slide 9.</i> </p> <p style="text-align: center; margin-top: 20px;">         The Arteris NoC in the Snapdragon SoC included in the Motorola product is a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks.     </p>

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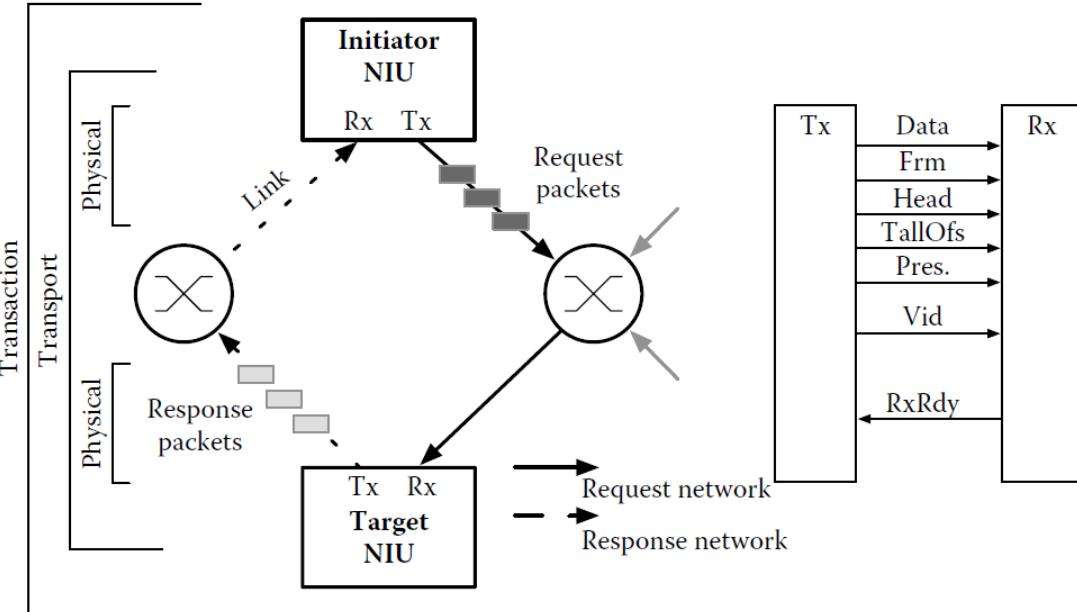
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	<p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p> <p><b>11.3.1.1 <i>Transaction Layer</i></b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv1f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv1f0</a>, at 311, 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p><b>FIGURE 11.1</b>  NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 312.</p>

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each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,	<p>In the Arteris NoC utilized by the Snapdragon SoC included in the Motorola product, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, either literally or under the doctrine of equivalents.</p> <p>For example, the "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes":</p> <p><b>11.3.1.2 Transport Layer</b></p> <p>The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 313.</p> <p>As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals":</p>

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maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in [Figure 11.1](#)) defines the following signals:

- **Data**—Data word of the width specified at design-time.
- **Frm**—When asserted high, indicates that a packet is being transmitted.
- **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.
- **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.
- **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in [Figure 11.2](#)).
- **Vld**—Data valid: when asserted high, indicates that a word is being transmitted.
- **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy.

This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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	Field	Size	Function
	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
	MstAddr	User Defined	Master address
	SlvAddr	User Defined	Slave address
	SlvOfs	User Defined	Slave offset
	Len	User Defined	Payload length
	Tag	User Defined	Tag
	Prs	User defined (0 to 2)	Pressure
	BE	0 or 4 bits	Byte enables
	CE	1 bit	Cell error
	Data	32 bits	Packet payload
	Info	User Defined	Information about services supported by the NoC
	Err	1 bit	Error bit

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	<table> <tr> <td>StartOfs</td> <td>2 bits</td> <td>Start offset</td> </tr> <tr> <td>StopOfs</td> <td>2 bits</td> <td>Stop offset</td> </tr> <tr> <td>WrpSize</td> <td>4 bits</td> <td>Wrap size</td> </tr> <tr> <td>Rsv</td> <td>Variable</td> <td>Reserved</td> </tr> <tr> <td>CtlId</td> <td>4 bits/3 bits</td> <td>Control identifier, for control packets only</td> </tr> <tr> <td>CtlInfo</td> <td>Variable</td> <td>Control information, for control packets only</td> </tr> <tr> <td>EvtId</td> <td>User defined</td> <td>Event identifier, for event packets only</td> </tr> </table>		StartOfs	2 bits	Start offset	StopOfs	2 bits	Stop offset	WrpSize	4 bits	Wrap size	Rsv	Variable	Reserved	CtlId	4 bits/3 bits	Control identifier, for control packets only	CtlInfo	Variable	Control information, for control packets only	EvtId	User defined	Event identifier, for event packets only
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	<p>The diagram illustrates the NTTP (Network-on-Chip Transport Protocol) packet structure. It shows two header formats: Necker and Data, followed by a series of data bytes.</p> <ul style="list-style-type: none"> <li><b>Necker Header:</b> This header is 35 bits long. It includes fields for Info (29-28), Len (25-24), Master Address (20-15), Slave Address (14-13), Prs (5-4), and Opcode (3-0). The Info field is divided into Tag (29) and Err (28). The Master Address and Slave Address fields are 6-bit fields. The Prs and Opcode fields are 2-bit fields. The Data field is 24 bits long and contains multiple BE (Byte-Enable) and Data Byte fields.</li> <li><b>Data Header:</b> This header is 32 bits long. It includes fields for Rsv (31), Len (30), Info (27-26), Tag (20-19), Master Address (14-13), Prs (5-4), and Opcode (3-0). The Rsv field is 1 bit, Len is 2 bits, Info is 2 bits, Tag is 2 bits, Master Address is 6 bits, Prs is 2 bits, and Opcode is 2 bits. The Data field is 20 bits long and contains multiple CE (Content-Enable) and Data fields.</li> <li><b>Data Payload:</b> Following the headers, there are multiple data bytes. The first Data row shows a sequence of BE and Data Byte fields. The second Data row shows a sequence of BE and Data Byte fields. The third Data row shows a sequence of CE and Data fields.</li> </ul>																						

**FIGURE 11.2**  
NTTP packet structure.

Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 313, 314-315.

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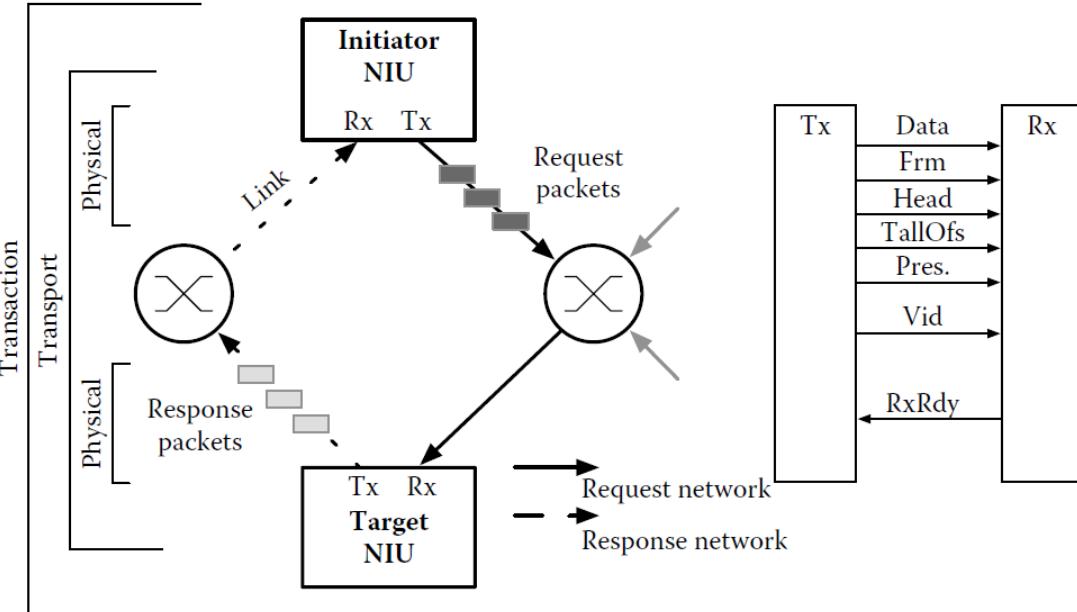
'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>
the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface,	<p>In the Arteris NoC utilized by the Snapdragon SoC included in the Motorola product, the plurality of network stations comprise a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p> <p><b>11.3.1.1 Transaction Layer</b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p> <p><i>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 311, 312-313.</i></p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

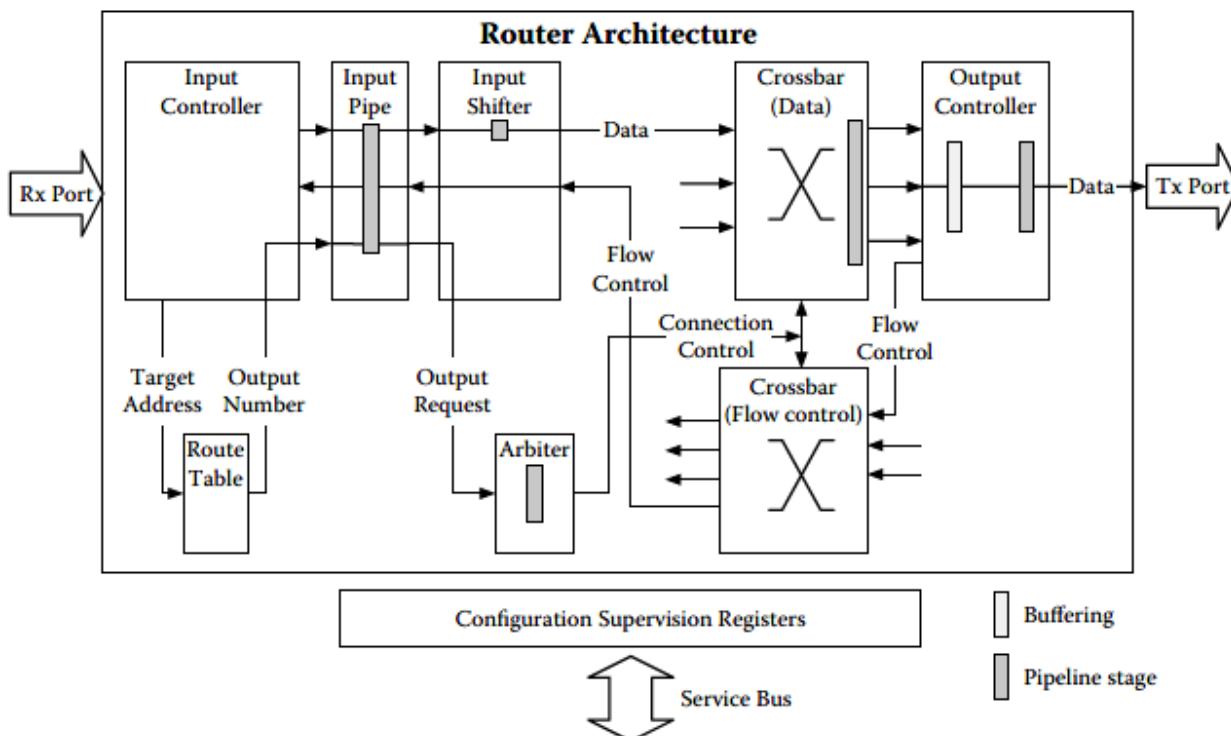
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'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>
	 <p><b>FIGURE 11.1</b>  NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 312.</p> <p>As a further illustration of the routers in the Arteris NoC:</p>

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### 11.3.3.2 *Routing*

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address



**FIGURE 11.6**  
 Packet transportation unit: Router architecture.

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	<p>As a further illustration of the network interfaces in the Arteris NoC:</p> <p><b>11.3.2.1 Initiator NIU Units</b></p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 317.</p>

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	<p><b>11.3.2.2 Target NIU Units</b></p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, <a href="#">Figure 11.2</a>). The AHB address bus is always</p> <p><i>Id.</i> at 318.</p>
<p>the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication</p>	<p>In the Arteris NoC utilized in the Snapdragon SoC included in the Motorola product, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising <math>M^*N</math> data storage elements, <math>M</math> being a positive integer, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p>

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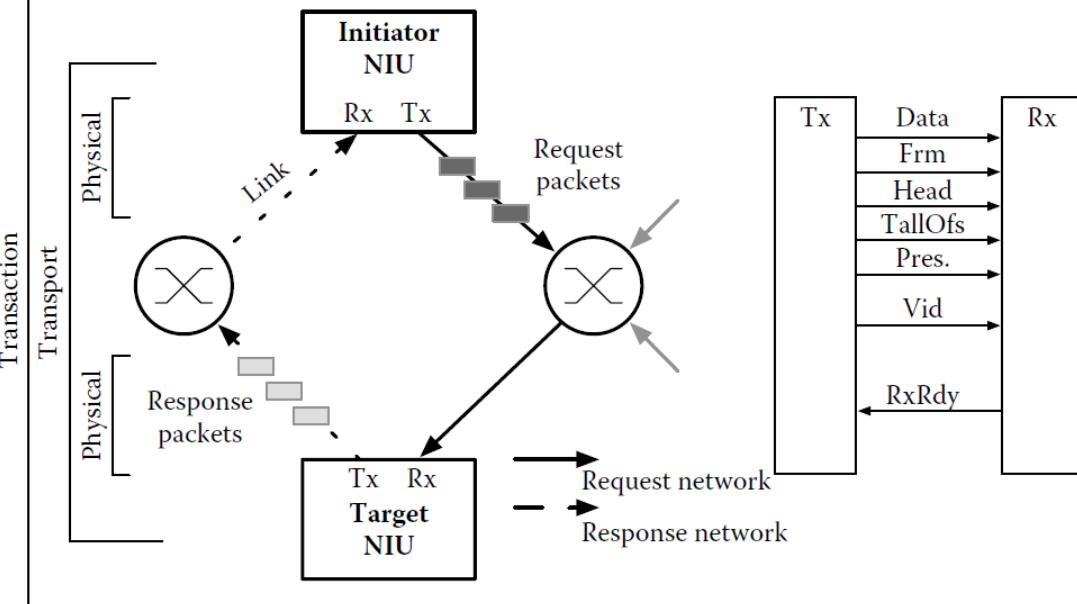
'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>
network further comprising $M^*N$ data storage elements, $M$ being a positive integer,	<p><b>11.3.1.1 <i>Transaction Layer</i></b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	<p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 311, 312-313.</p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p><b>FIGURE 11.1</b>  NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 312.</p> <p>As a further example, a “delay pipeline is automatically inserted in the input controller to keep data and routing information in phase” and an input pipe “introduces a one-word-deep FIFO”:</p>

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	<p>Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the</p> <p style="text-align: center;">* * *</p> <p>The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle.</p> <p><i>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 322.</i></p> <p>As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element “with as many words as there are date pipelined in the crossbar”:</p>

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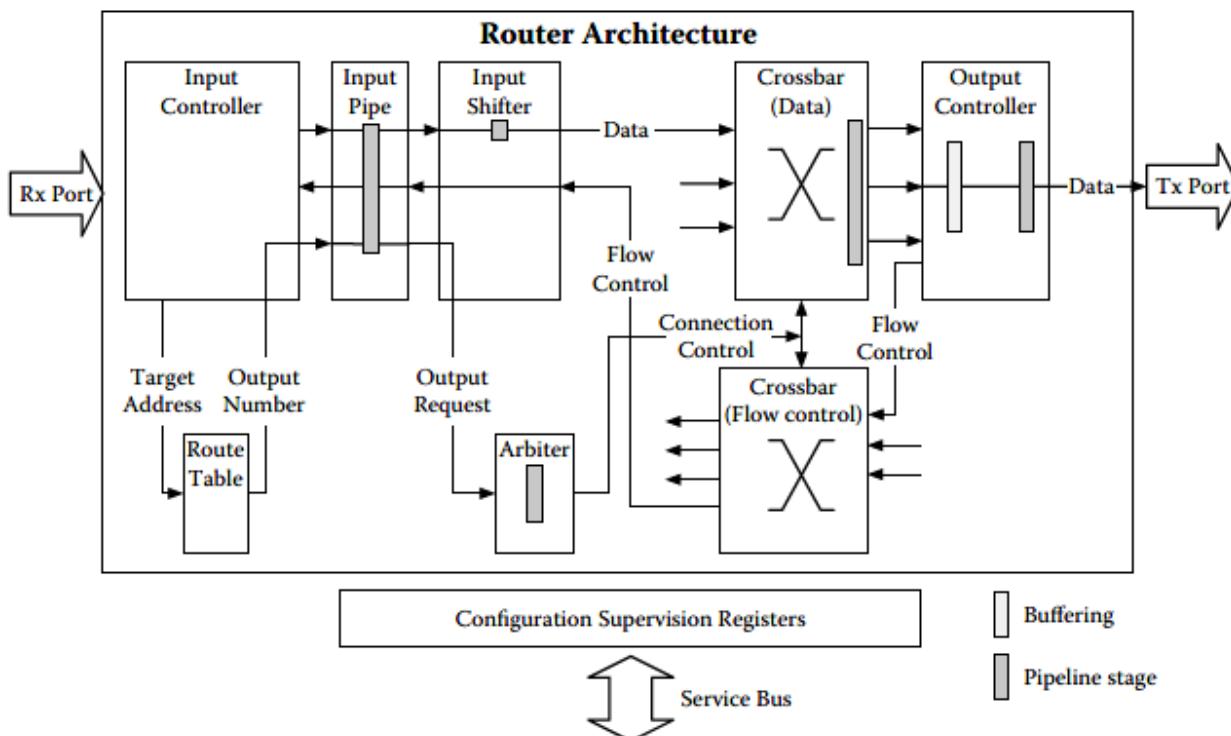
“Integrated circuit with data communication network and IC design method”

'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip <sup>1</sup>
	<p>The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of <math>m</math> muxes (one per output port), each having <math>n</math> inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as <math>\max(n, m)</math>.</p> <p>The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller.</p> <p><i>Id.</i> at 323.</p> <p>The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:</p>

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### 11.3.3.2 *Routing*

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address



**FIGURE 11.6**  
 Packet transportation unit: Router architecture.

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	<p><i>Id.</i> at 320.</p> <p>As another example, the “fwdPipe” parameter “introduces a true pipeline register on the forward signals” and “inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path”:</p> <p style="padding-left: 40px;">get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path.</p> <p><i>Id.</i> at 323-324.</p>
the data communication introducing a delay of M*N cycles on the first communication channel when the data communication	<p>In the Arteris NoC utilized in the Snapdragon SoC included in the Motorola product, the data communication introducing a delay of M*N cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold, either literally or under the doctrine of equivalents.</p> <p>For example, a “delay pipeline is automatically inserted in the input controller to keep data and routing information in phase” and an input pipe “introduces a one-word-deep FIFO”:</p>

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<p>network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.</p>	<p>Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the  * * *</p> <p>The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 322.</p> <p>As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element "with as many words as there are date pipelined in the crossbar":</p>

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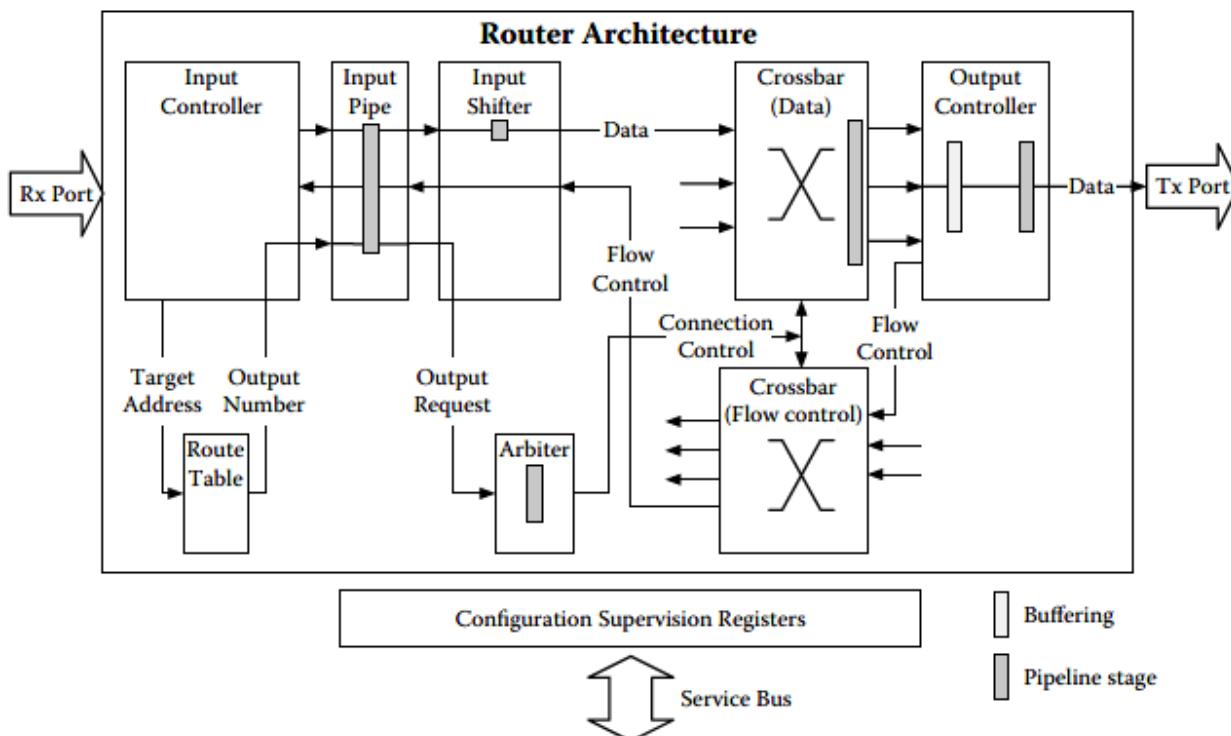
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	<p>The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of <math>m</math> muxes (one per output port), each having <math>n</math> inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as <math>\max(n, m)</math>.</p> <p>The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller.</p> <p><i>Id.</i> at 323.</p> <p>The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:</p>

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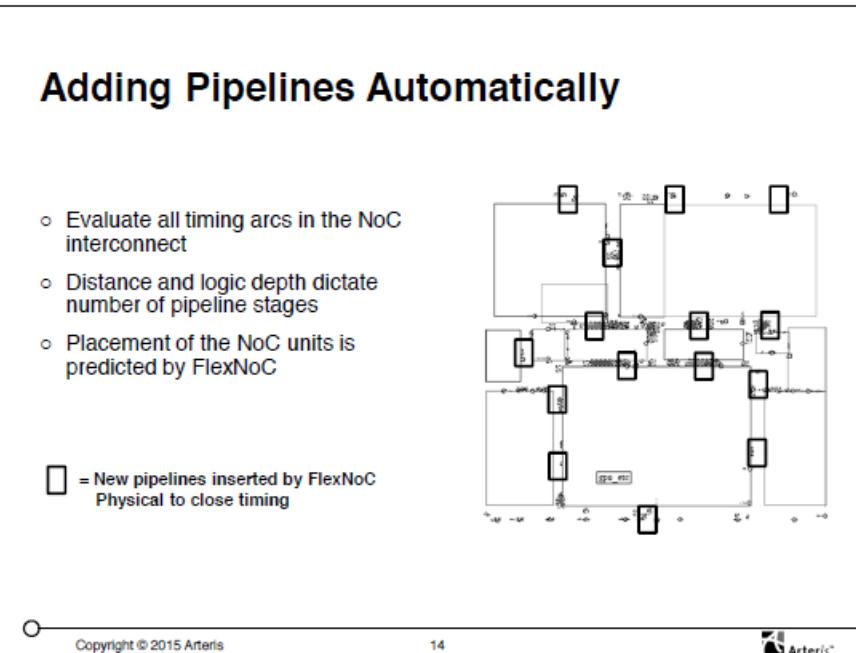
**FIGURE 11.6**  
 Packet transportation unit: Router architecture.

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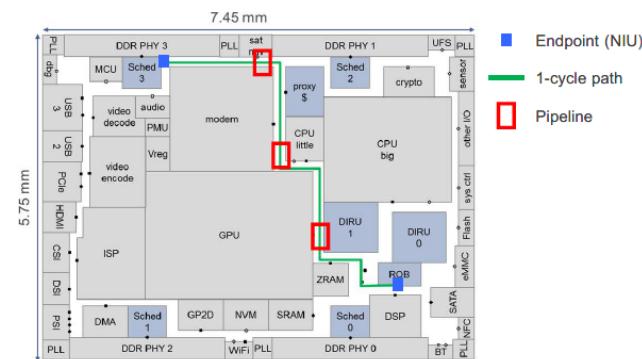
“Integrated circuit with data communication network and IC design method”

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	<p><i>Id.</i> at 320.</p> <p>As another example, the “fwdPipe” parameter “introduces a true pipeline register on the forward signals” and “inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path”:</p> <p style="padding-left: 40px;">get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path.</p> <p><i>Id.</i> at 323-324.</p> <p>As another example, pipelines may be automatically inserted by the Arteris NoC to close timing:</p>

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	<p style="text-align: center;"><b>Adding Pipelines Automatically</b></p> <ul style="list-style-type: none"> <li>○ Evaluate all timing arcs in the NoC interconnect</li> <li>○ Distance and logic depth dictate number of pipeline stages</li> <li>○ Placement of the NoC units is predicted by FlexNoC</li> </ul> <p></p> <p> Copyright © 2015 Arteris</p> <p style="text-align: center;">14</p> <p style="text-align: right;"> Arteris® The Network for SoC Success</p> <p>Using SoC Interconnect IPs to Improve Physical Layout, <a href="http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf">http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf</a>, at slide 14.</p> <p>As a further illustration, the Arteris NoC includes pipelining for distance spanning when traveling “~6mm” has a propagation delay of “~400ps/mm”, requiring at least “2400ps to span the Distance”; thus requiring “at least 3 pipeline stages and 4 clock cycles to meet timing.”</p>

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	<h2 data-bbox="530 306 1727 367">Wire Delays – Can't Cross a Chip in 1 Clock Cycle</h2> <p data-bbox="530 372 1417 399">PHYSICAL DISTANCE DICTATES THE NUMBER OF PIPELINE STAGES</p> <div style="display: flex; align-items: center;">  <p data-bbox="692 652 882 682">Clock Cycles</p> </div> <ul data-bbox="530 750 1522 889" style="list-style-type: none"> <li>• Interconnect Frequency: 1.2GHz = 833ps</li> <li>• Distance to travel = ~6mm</li> <li>• Propagation delay = ~400ps/mm in 16nm FinFET; Needs 2400ps to span the distance</li> <li>• Requires at least 3 pipeline stages and 4 clock cycles to meet timing</li> </ul> <div data-bbox="530 905 1803 966" style="background-color: #ff7043; color: white; padding: 5px; border-radius: 5px;"> <p data-bbox="530 905 1803 966">Large 14nm FinFET SoC may have &gt;6,000 pipelines with 6K factorial pipeline combinations and 60 timing parameters – Too much for human comprehension!</p> </div> <div data-bbox="1184 425 1826 784" style="margin-top: 20px;">  <p data-bbox="1184 425 1826 784"> <span style="color: blue;">█</span> Endpoint (NIU)  <span style="color: green;">—</span> 1-cycle path  <span style="color: red;">█</span> Pipeline     </p> </div> <div data-bbox="506 995 639 1023" data-label="Text">ARTERIS IP</div> <div data-bbox="1094 998 1248 1018" data-label="Text">ISPD 2018, 28 March 2018</div> <div data-bbox="1626 998 1848 1018" data-label="Text">Copyright © 2018 Arteris IP   3</div> <p data-bbox="466 1052 1854 1132">See Physical Interconnect Aware Network Optimizer, <a href="http://www.ispd.cc/slides/2018/s7_2.pdf">http://www.ispd.cc/slides/2018/s7_2.pdf</a>, at slide 3.</p>